

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/808,705
 Priority Filing Date March 14, 2001
 Inventor Shubneesh Batra et al.
 Assignee Micron Technology, Inc.
 Priority Group Art Unit 2823
 Priority Examiner H.M. Lee
 Attorney's Docket No. MI22-2397
 Title: Methods of Forming Polished Material and Methods of Forming Isolation Regions

INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/808,705, filed March 14, 2001, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). A copy of the cited article is enclosed for the Examiner's reference.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 9-24-03



D. Brent Kenady
 Reg. No. 40,045

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2397	SERIAL NO.	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Shubneesh Batra et al.		
				FILING DATE filed herewith	GROUP	
U.S. PATENT DOCUMENTS						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,728,621	03/98	Zheng et al.		
	AB	5,834,358	11/98	Pan et al.		
	AC	5,923,993	07/99	Sahota		
	AD	5,817,567	10/98	Jang et al.		
	AE	5,387,539	02/95	Yang et al.		
	AF	5,915,190	06/99	Pirkle		
	AG	5,930,646	07/99	Gerung et al.		
	AH	5,665,202	09/97	Subramanian et al.		
	AI	5,459,096	10/95	Venkatesan et al.		
	AJ	5,904,539	05/99	Hause et al.		
	AK	5,872,045	02/99	Lou et al.		
FOREIGN PATENT DOCUMENTS						
	Document Number	Date	Country	Class	Subclass	Translation
						Yes No
	AL					
	AM					
	AN					
	AO					
	AP					
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)						
	AR		S. Wolf, Silicon Processing for the VLSI Era, Volume 2 - Process Integration (Published by Lattice Press, Copyright 1990) (pgs. 229-232)			
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U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	5,435,888	07/95	Kalniisky et al.				
AB	6,274,498	08/01	Moore et al.				
AC	4,656,497	04/87	Rogers et al.				
AD	5,735,335	04/98	Gilmore et al.				
AE	5,920,792	07/99	Lin				
AF	4,769,340	09/88	Chang et al.				
AG	5,759,913	06/98	Fulford, Jr. et al.				
AH							
AI							
AJ							
AK							
FOREIGN PATENT DOCUMENTS							
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